# New Design Method of Non-Uniform Distributed Power Amplifiers. Application to a single stage 1W PHEMT MMIC.

C. Duperrier*, M. Campovecchio*, L. Roussel**, M. Lajugie**, R.Quere*

*IRCOM, UMR CNRS n°6615, 123 avenue Albert Thomas, 87060 Limoges, France.
**THALES MICROWAVE, 29 av. Carnot, 91349 Massy, France.

***Abstract* — A new design methodology of non-uniform distributed power amplifiers is reported in this paper. This method is based on analytical expressions of the optimum input and output artificial lines making up the non-uniform distributed power amplifier. These relationships are based on the optimum load line requirement for power operation. To validate the proposed design methodology, a non-uniform distributed power amplifier has been manufactured at the TriQuint Semiconductor foundry using a 0.25µm power PHEMT process. This single stage MMIC amplifier is made of six non-uniform cells and demonstrates 1W output power with 7dB associated gain and 20% PAE over multi-octave bandwidth.**

## I. Introduction

MMIC power amplifiers are highly necessary for broadband microwave communication systems and radars. Criteria like maximum power and maximum efficiency, but also high reliability and high integration, are the most important issues.

Distributed amplification has already demonstrated high performances for ultra broadband operation but its power behavior must be carefully optimized using suited design methodologies. The basic principle of distributed amplification overcomes the limitations related to finite gain-bandwidth product by paralleling devices so that their gate and drain capacitances are absorbed into artificial transmission lines. Unfortunately, several power-limiting mechanisms can be identified within distributed amplifiers. Indeed, each transistor demonstrates a strongly frequency-dependent power behavior so that the overall output power is only a small fraction of the combined power capabilities of all active devices [1].

A design methodology of non-uniform distributed power amplifiers is proposed in this paper. This work is a generalization of our previously published design method of uniform distributed amplifiers [2]. The design parameters of artificial gate and drain lines are expressed as a function of the optimum power load of each FET size providing both the initial values and right directions in which the optimum trade-off can be reached between wide band and high power operation.

## II. Design Methodology of Non-Uniform Distributed Power Amplifiers

### A. *Optimum Power Load*

The first important step in all power amplifier designs is the determination of the optimum power load of the device that maximizes its output power. The optimum load can either be determined by nonlinear simulations or by load-pull measurement [3]. As generally confirmed by experimental results on FETs, the conjugate of the optimum power load is almost equivalent to a constant conductance $G_{OPT}$ in parallel with a constant capacitance $C_{OPT}$ over very wide bandwidths. Therefore, this optimum load can be used to design distributed power amplifiers with equal control voltages and optimum power loads seen by each active device. In the case of transistors T(i) with different gate widths, the optimum load will be called $(G_{OPT(i)}//C_{OPT(i)})$ in the following design relationships.

### B. *Drain Line*

Figure 1 shows the architecture of a non-uniform distributed amplifier where the n transistors of different sizes are called $T_{(i)}$. The optimum characteristic conductances of input and output transmission lines are respectively called $G_{CG(i)}$ and $G_{CD(i)}$ while the input and output dumping loads are respectively called $G_{GL}$ and $G_{DL}$. It should be noted that the optimum output capacitances $C_{OPT}(i)$ are absorbed into the artificial drain line to synthesize the required optimum characteristic conductances $G_{CD(i)}$.

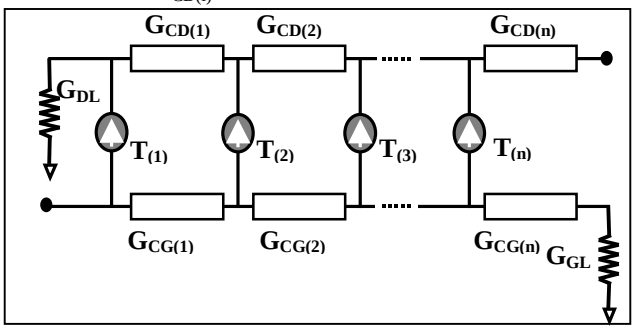


Fig.1: Non-uniform distributed power amplifier (n cells).

In the case of uniform distributed amplifiers, we have already determined and reported the analytical expressions giving the optimum characteristic conductances of the gate and drain lines [1-2]. In this paper, we report new generalized expressions giving the optimum characteristic conductances in the case of non-uniform distributed amplifiers (Fig.1).

For very wide bandwidths, the drain load $G_{DL}$ cannot be omitted. Consequently, the first device $T_{(1)}$ provides a reduced power $P_{OUT(1)}$ in comparison with its maximum output power capability $P_{max(1)}$. Nevertheless, in the same manner as previously described for the uniform distributed architecture [1-2], the characteristic conductances $G_{CD(i)}$ can be successively determined so that the other transistors $T_{(i\geq 2)}$ supply their maximum output power $P_{max(i)}$. Finally, the generalized optimum power matching structure is determined to add the individual power contributions in the direction of the output port.

$$G_{CD(1)} = G_{OPT(1)} \tag{1}$$

$$G_{CD(i\geq 2)} = \left( \frac{G_{OPT(1)}{}^{2}}{G_{DL} + G_{OPT(1)}} + \sum_{k=2}^{i} G_{OPT(k)} \right) \tag{2}$$

$$P_{OUT(1)} = \left( \frac{G_{OPT(1)}}{G_{DL} + G_{OPT(1)}} \right) \cdot P_{\max(1)} \tag{3}$$

$$P_{OUT} = P_{OUT(1)} + \sum_{k=2}^{n} P_{\max(k)} \tag{4}$$

where $Gopt_{(k)}$ and $Pmax_{(k)}$ are respectively, the optimum output conductance and output power of the $k^{th}$ transistor $T_{(k)}$ while $G_{DL}$ is the dumping drain load, $G_{CD(i)}$ is the optimum characteristic conductance of the $i^{th}$ drain line and $P_{OUT}$ is the overall output power (Fig.1).

It should be noted that in the case of moderate bandwidth applications, the dumping load $G_{DL}$ can be omitted so that each FET is matched on its optimum power load and yields its maximum output power.

$$G_{CD(i)} = \sum_{k=1}^{i} G_{OPT(k)} \quad ; \quad P_{OUT} = \sum_{k=1}^{n} P_{\max(k)} \tag{5}$$

### C. Gate Line

In the same manner as in the drain line case, the optimum characteristic conductances $G_{CG(i)}$ of the gate line can be determined to match the input equivalent conductances $G_{IN(i)}$ of transistors $T_{(i)}$ so that equal gate voltage amplitudes can be obtained over the frequency band. The equivalent input capacitances $C_{IN(i)}$ are absorbed into the artificial gate line to synthesize the required optimum characteristic conductances $G_{CG(i)}$.

To achieve the equal gate voltage condition, the characteristic conductances are given by:

$$G_{CG(i)} = \sum_{k=i}^{n} G_{IN(k)} \quad ; \quad G_{GL} = G_{IN(n)} \tag{6}$$

It should be noted that the input equivalent conductances $G_{IN(i)}$ are frequency dependent, which makes the gate matching accurate at a single frequency. However, when the characteristic conductances $G_{CG(i)}$ are determined at the maximum operating frequency, almost constant gate voltage amplitude can be reached over a wide frequency band.

Moreover, in order to meet the condition of equal phase velocity on the gate and drain lines, the electrical lengths $\theta_{CG(i)}$ and $\theta_{CD(i)}$ of the corresponding gate and drain line sections must verify:

$$\theta_{CG(i)} = \theta_{CD(i)} \tag{7}$$

Finally, improved output power performances can be achieved by using non-uniform distributed power amplifiers with tapered gate and drain artificial lines following the power load constraints expressed by the preceding relationships.

## III. Application to a Single Stage MMIC Amplifier

A non-uniform distributed power amplifier has been designed in cooperation with Thomson laboratories following this specific design procedure. The MMIC circuit has been manufactured using a 0.25µm power pHEMT process from the TriQuint foundry. The single stage amplifier architecture integrates six amplifying cells (Figure 2). The first transistor $T_{(1)}$ is a 600µm pHEMT while the other transistors T(i≥2) are 300µm pHEMT.

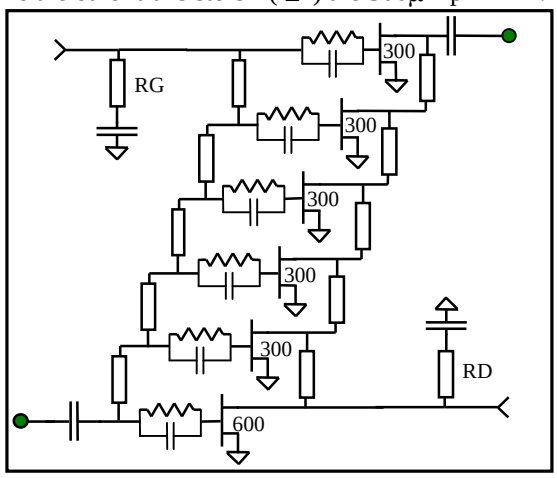

Fig. 2: Schematic of the non-uniform distributed amplifier.

In this case, the preceding optimum relationships of drain line characteristic admittances can be simplified using the following assumptions:

$$G_{OPT(1)} = G_{OPT(600\mu m)} \approx 2 \cdot G_{OPT(300\mu m)} \quad (8)$$

$$G_{OPT(i\geq 2)} = G_{OPT(300\mu m)} \quad (9)$$

*A. Nonlinear Modeling and Design Process*

In a first step, the 300µm and 600µm devices have been modeled using pulsed I-V and pulsed S-parameter measurements. Then, the optimum power loads provided by the foundry were compared to nonlinear simulation results. Finally, the optimum power load of the 300µm and 600µm devices have been found sensibly constant and respectively equal to (10ms, -0.18pF) and (18ms, -0.31pF) in the frequency band.

Uniform and non-uniform distributed amplifiers were initially designed with the aim to supply 1W output power and 20% PAE over multioctave bandwidth. In this case, it has been found that a non-uniform distributed architecture (1st device of double gate width) offers the best trade-off between the output power, the gain and the return losses. Therefore, given the preceding optimum power loads, the tapered drain line has been optimized so that the first 600µm device supplies a reduced output power but enables the five following 300µm devices to be ideally power matched. Figure 3 shows the obtained simulated load lines of each device at $f_{min}$ and $f_{max}$. In accordance with theory, it can be observed that the first device is affected by the dumping drain load and is not well matched but enables the other devices to be quite ideally power matched.

The optimum tapered gate line has been obtained through a gate coupling capacitor profile along the input line (Fig.2). Discrete series capacitors couple each active device to the input line and act as voltage dividers so that to ensure equal drive levels on the transistor gates [4]. Implanted GaAs resistors shunt the series MIM capacitors to supply gate bias.

*B. Circuit Realization and Measured Performances*

The non-uniform distributed power amplifier has been manufactured at the TriQuint MMIC foundry using a 100µm-thick GaAs substrate and 0.25µm power pHEMTs. The main electrical parameters of this wideband process are typically 295mA/mm saturated current, -1V pinchoff voltage and more than 16V breakdown voltage for an associated power density of 800mW/mm.

The final circuit layout is shown on Figure 4. It should be noted that the smallest values of gate coupling capacitances have been synthesized by two series capacitors in order to meet the minimum size condition on MIM capacitors.

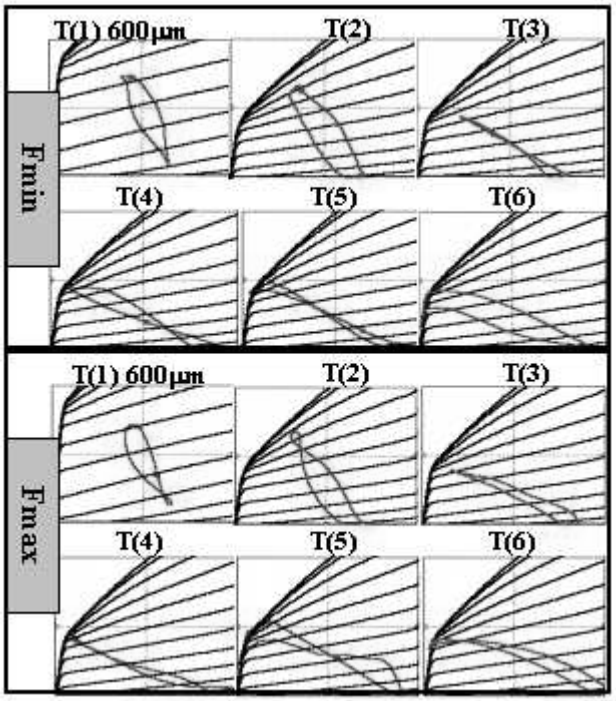


Fig.3: Simulated device load lines at $f_{min}$ and $f_{max}$ [ T(1)=600µm and T(2→6)=300µm ]

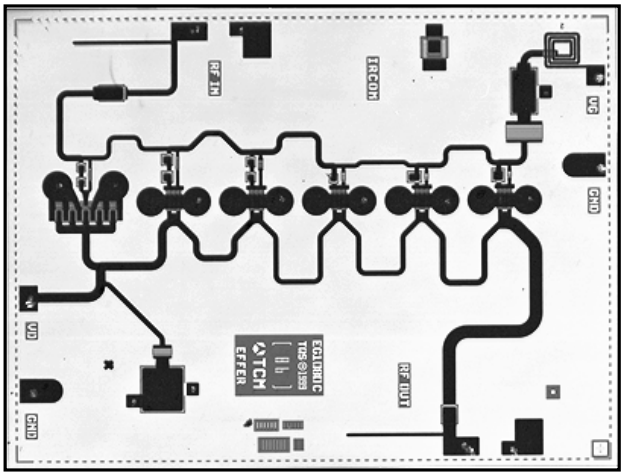


Fig.4: Non-uniform MMIC distributed power amplifier.

After wafer manufacturing, the non-uniform distributed amplifier was tested for DC operation and RF performances in class A operation (Vds=8V, Ids=270mA). The figure 5 shows a comparison between small-signal on-wafer measurements and simulations in the frequency band. A good agreement is obtained for input and output return losses that are lower than –10dB in all the bandwidth. The measured linear gain is 1dB less than the simulated one and lies around 8.5dB before decreasing to 7dB at the highest frequency.

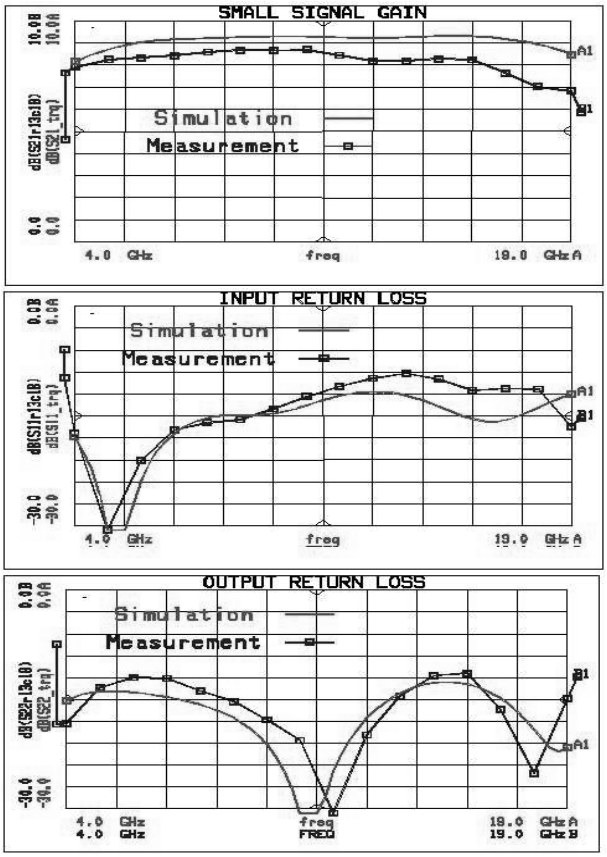


Fig. 5: Simulations and typical on-wafer measurements of small-signal gain and return losses.

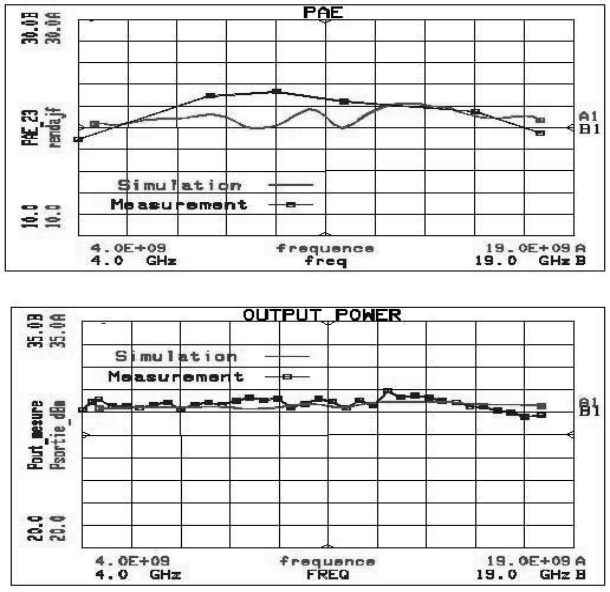


Fig. 6: Simulated and measured PAE and output power @ Pin=23dBm, Vds=8V and Ids=270mA.

At an input power of 23dBm, on-wafer CW power measurements exhibited 29dBm output power. Test fixture measurements have also been performed. The MMIC circuit was soldered on a Mo carrier and interfaced to the RF connectors with 13mm long 50Ω microstrip alumina lines. The measured circuit exhibited 30dBm CW output power and more than 20% power added efficiency. Figure 6 shows the good agreement obtained between predicted and measured output power and PAE.

All these results have been obtained after one foundry pass and without circuit tuning.

## IV. Conclusion

A new design methodology of non-uniform distributed power amplifiers is reported in this paper. This method is a generalization of our previously published work on uniform distributed amplifier [2]. It is based on analytical expressions of the optimum input and output artificial lines making up the non-uniform distributed amplifier. These relationships are based on the optimum power load of each device size in the frequency band. To validate the proposed design methodology, a non-uniform single stage distributed power amplifier has been designed and manufactured at the TriQuint Semiconductor foundry using a 0.25µm pHEMT process. After one foundry pass, this MMIC amplifier has demonstrated 1W output power with 7dB associated gain and a minimum of 20% PAE over multi-octave frequency band.

## ACKNOWLEDGEMENTS

Thanks to French DGA/DSP/STTC for supporting this work.

## References

[1] M. Campovecchio, B. Le Bras, M. Lajugie and J. Obregon, "Optimum design of distributed power FET amplifiers. Application to 2-18 GHz MMIC module exhibiting improved power performances" *IEEE MTT-S Digest, pp. 125-128*, San Diego, 1994.

[2] M Campovecchio, B. Le Bras, R. Hilal, M. Lajugie and J. Obregon "Large signal design method of distributed power amplifiers applied to a 2 to 18 GHz GaAs chip exhibiting high power density performances" *International Journal of Microwave and Millimeter-Wave Computer-Aided Engineering*, vol. 6 n°4, pp. 259-269, 1996.

[3] F. Blache, J.M. Nebus, P. Bouysse, J.P. Villotte "A novel computerized multiharmonic active load-pull system for the optimization of high efficiency operating classes in power transistors" *IEEE MTTS-Digest*, pp 1037-1040, 1995.

[4] Y. Ayasli, S.W. Miller, R. Mozzi, L.K. Hanes "Capacitively coupled travelling wave power amplifier" *IEEE Trans. on MTT, Vol. 32*, pp 1692-1700, Nov. 1990.